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McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
GRAHAM, KRETELIA	
ART UNIT	**PAPER NUMBER**
2827	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/986,290	LANDFIELD ET AL.	
	Examiner	Art Unit	
	Kretelia Graham	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *5,6,9-11,18 and 19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,8 and 12-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/30/02, 10/4/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims 1-4, 7, 8, and 12-17 in the reply filed on 3/3/2006 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Objections

2. Claims 3, 4, 7, 8, and 12-14 are objected to because of the following informalities:

Pertaining to claim 3, the "array of fixed interconnected memory storage units" of **claim 3, line 1** lack proper antecedent basis.

Pertaining to claim 4, the Examiner suggests changing "devices" of **claim 4, lines 3 and 4** to "semiconductor devices" in order to properly reference the devices of **claim 3, line 2**. It is unclear as to whether the "array" of **claim 4, lines 5, 8, and 9** are referring to the linked array of **claim 4, line 3** or parallel arrays of **claim 1, line 3**. The claim limitations "...being responsive to pulse to latch..." of **claim 4, line 8** and "...being responsive to subsequent delayed pulse to latch..." of **claim 4, line 10** are unclear and should be re-worded for clarity.

Pertaining to claim 7, the Examiner suggests changing "units" of **claim 7, line 3** to "fixed memory storage units" in order to properly reference the storage units of **claim 1, line 3**.

Pertaining to claim 8, the Examiner suggests changing "array" of **claim 8, line 1** to "arrays" in order to properly reference the arrays of storage units of **claim 1, line 3**.

Pertaining to claim 12, it is unclear as to whether the "arrays of fixed memory storage units" of **claim 12, line 4** are intended to reference the arrays of **claim 12, line 2** or establish different arrays. The "corresponding time slices" of **claim 12, line 6** lack proper antecedent basis.

Pertaining to claim 13, the Examiner suggests changing "information" of **claim 13, line 3** to "temporally sequential information" in order to properly reference the sequential information of **claim 13, line 1**. The Examiner suggests changing "units" of **claim 13, lines 6 and 7** to "fixed memory storage units" in order to properly reference the storage units of **claim 13, line 3**. The "linked array" of **claim 13, line 7** lacks proper antecedent basis.

Pertaining to claim 14, The Examiner suggests changing "units" of **claim 14, line 3** to "fixed memory storage units" in order to properly reference the storage units of **claim 13, line 3**. The "spatial sequence" of **claim 14, line 3** lacks proper antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Pertaining to claim 17, the claim limitation "such devices" of **claim 17, line 6** renders the claim indefinite. It is unclear as to whether the "such devices" are referencing the "first semiconductor device" of **claim 17, line 5**, "first array of simultaneously activated devices" of **claim 17, line 5**, or "second semiconductor device" of **claim 17, line 5**.

It is unclear as to whether the "first semiconductor memory device" of **claim 17, line 9** is intended to reference the first semiconductor device of **claim 17, line 5** or establish another device.

The claim limitation "semiconductor memory device" of **claim 17, line 10** renders the claim indefinite. It is unclear as to whether the "semiconductor memory device" is referencing the device of **claim 17, line 5 or line 9**.

It is unclear as to whether the "second semiconductor memory device" of **claim 17, line 13** is intended to reference the second semiconductor device of **claim 17, line 6** or establish another device.

The claim limitation "transmitting the delayed pulse or second pulse to a second semiconductor memory device or array, adjacent functionally to the first semiconductor

memory device, said second semiconductor memory device or array..." of **claim 17, lines 13-15** render the claim indefinite. The Examiner is uncertain of the relationship between the first device, second device, and array.

The claim limitation "first semiconductor memory device" of **claim 17, line 14** renders the claim indefinite. It is unclear as to whether the first semiconductor memory device is referencing the device of **claim 17, lines 5 or 9**.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-4, 7, 8, and 12-17 are rejected under 35 U.S.C. 102(e) as being anticipated by the US patent to Brown (6,351,427 B1), hereafter "Brown".

Pertaining to claim 1, **FIG. 4** is directed towards: A memory **400** for storing temporally sequential information **data in data input/output 430 (see column 7, lines 52-54)** that is not a serial sequential access memory **Note: Data is accessed in a parallel manner and not serially (see column 6, lines 45-53)**, comprising: parallel arrays of fixed memory storage units **402a-402n; see column 6, lines 56-58**; means for applying **434, 424, 426** the temporally sequential information to the array of fixed

memory storage units; and means for successively activating **440,448** each of the fixed memory storage units or linked arrays of said units in sequence to store or retrieve corresponding time slices of the temporally sequential information **Note: See FIG. 5 where bank control signals BANK0, BANK1 are sequentially activated to indicate which particular memory array is being accessed**.

Pertaining to claim 2, **FIG. 4** is directed towards: wherein the temporally sequential information is applied along parallel inputs **Note: Since the data is accessed in parallel it is inherent that parallel inputs be used to transmit the data (see column 6, lines 45-53)** to multiple temporally linked arrays **memory cell arrays in each bank 402a-402n (see column 6, lines 56-58)** of fixed memory storage units, such that units in one array are activated to store information of the parallel inputs at one point in time, whereas units in other arrays are successively enabled to store information from the same parallel inputs at subsequent sequential points in time **Note: See FIG. 5 where bank control signals BANK0, BANK1 are sequentially activated to indicate which particular memory array is being accessed for a read/write operation**.

Pertaining to claim 3, **FIG. 4** is directed towards: wherein the array of fixed interconnected memory storage units includes semiconductor memory devices.

Pertaining to claim 4, **FIG. 4 and FIG. 10** are directed towards: said means for applying includes an input bus or buses **424,426** coupled to inputs of a first semiconductor memory device of linked array of said devices, and a second semiconductor memory device, or linked array of said devices, adjacent functionally to

the first semiconductor memory device of array; and wherein said means for successively activating includes a pulse generator **448** for generating a pulse **SHFTCLK** that enables storage of input data **see column 8, lines 28-38** and a delay clock element for delaying the enabling pulse **see column 14, lines 52-59**, said first semiconductor memory device or array being responsive to pulse to latch data presented at inputs thereof and said second semiconductor memory device or array being responsive to subsequent delayed pulse to latch data presented at inputs thereof.

Pertaining to claim 7, **FIG. 4** is directed towards: means for successively activating each of the fixed memory storage units or interconnected arrays of said units in the same temporal sequence in which they were activated during storage to retrieve the corresponding time slices of the temporally sequential information **Note: Memory device 400 operates as shown in FIG. 3 when a "same bank" write-followed-by-read operation is done, in which a read and write operation are performed during the same cycle in which a bank selects signal BANK0, BANK1 is active**.

Pertaining to claim 8, **FIG. 4** is directed towards: wherein the array of fixed memory storage units includes semiconductor memory devices.

Pertaining to claim 12, **FIG. 4** is directed towards: A method for retrieving temporally sequential information **data in data input/output 430 (see column 7, lines 52-54)** comprising: arrays of fixed memory storage units **402a-402n; see column 6, lines 56-58**; means for applying **434, 424, 426** the temporally sequential information in a specified spatial sequence of arrays of fixed memory storage units; and means for successively activating **440** each of the fixed memory storage units in the spatial

sequence to retrieve the corresponding time slices of the temporally sequential information **Note: See FIG. 5 where bank control signals BANK0, BANK1 are sequentially activated to indicate which particular memory array is being accessed for a read/write operation**.

Pertaining to claim 13, **FIG. 4** is directed towards: A method for storing temporally sequential information **data in data input/output 430 (see column 7, lines 52-54)** in an array of fixed memory storage units, comprising the steps of: applying the information to spatially distinct array of fixed memory storage units**402a-402n; see column 6, lines 56-58**; and successively activating each of the fixed memory storage units or simultaneously activated arrays of said units in sequence to store a corresponding time slice of the temporally sequential information, one time slice in each unit or linked array **Note: See FIG. 5 where bank control signals BANK0, BANK1 are sequentially activated to indicate which particular memory array is being accessed for a read/write operation**.

Pertaining to claim 14, **FIG. 5** is directed towards: successively activating each of the fixed memory storage units or simultaneously activated arrays of said units in the spatial sequence to retrieve the corresponding time slices of the temporally sequential information **Note: See FIG. 5 where bank control signals BANK0, BANK1 are sequentially activated to indicate which particular memory array is being accessed for a read/write operation**.

Pertaining to claim 15, **FIG. 4** is directed towards: wherein the step of applying includes the step of applying the temporally sequential information to the arrays of fixed

memory storage units in parallel lines or waves **Note: Since the data is accessed in parallel it is inherent that parallel inputs be used to transmit the data (see column 6, lines 45-53)**.

Pertaining to claim 16, **FIG. 4** is directed towards: wherein the arrays of fixed memory storage units include semiconductor memory devices.

Pertaining to claim 17, **FIG. 4** is directed towards: the step of applying the temporally sequential information to the array of fixed memory storage units includes the steps of: applying the temporally sequential information to an input bus **424** that is coupled to inputs of a first semiconductor memory device or to a first array of simultaneously activated devices and a second semiconductor memory device or second array of such devices; and the step of successively activating each of the fixed memory storage units or array of said units in sequence includes the steps of: transmitting a pulse **BANK0** to a first semiconductor memory device or array **402a**, said first semiconductor memory device or array being responsive to the pulse to latch data presented at inputs thereof **Note: When signal BANK0 is activated memory array 402a is activated to store data during a write operation**; delaying or incrementing the pulse **see FIG. 5 where signal BANK1 is activated after signal BANK0**; and transmitting the delayed or second pulse to a second semiconductor device or array thereof, adjacent functionally to the first semiconductor memory device, said second semiconductor memory device or array, said second semiconductor memory devices or array being responsive to the delayed or incremented second pulse to latch data

presented at inputs thereof **Note: When signal BANK0 is activated memory array 402a is activated to store data during a write operation.**

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kretelia Graham whose telephone number is (571) 272-5055. The examiner can normally be reached on Mon-Fri 8am-4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KG
KG

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800